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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/897,902	HAYASHI ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 July 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. In this case, the title of the abstract is "ABSTRACT OF SAID DISCLOSURE", which includes the legal phraseology "said".

Claim Objections

3. Claims 3, 5-7, 9 and 11-14 are objected to because of the following informalities:

Substitute "A microprocessor" in line 1of the claims 3, 5, 6, 7 and 14, by --The microprocessor--, respectively.

Substitute "A semiconductor module" in line 1 of claim 9, by --The semiconductor module--.

Substitute "A data-processing system" in line 1 of claims 11-13, by --The data-processing system--, respectively.

Substitute "applies" in line 11 of claim 13, by --apply--.

In the claim 6, lines 7-8 and in the claim 7, line 3, they recite the subject matter "said clock signal", respectively. However, it is not clear that the subject matter "said clock signal" particularly points out either the subject matter "said first clock signal" or the subject matter "said second clock signal" in the parent claim 2. The Examiner assumes the subject matter "said clock signal" particularly points out the subject matter "said first clock signal" for the purpose of the claim rejection based on a prior art.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for generating the first clock signal and the second clock signal with a period equal to a predetermined multiple of the period of the first clock signal, the third clock signal and the fourth clock signal with a period equal to another predetermined multiple of the period of the third clock signal, and being each of the frequencies of the third and fourth clock signals at least equal to that of the first clock signal (See Application, page 9, line 15 through page 10, line 2), does not reasonably provide enablement for being each of the frequencies of the third and fourth clock signals equal to that of the first clock signal. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. The Examiner doubts how said each of frequencies of said third and fourth clock signals could be that of said first clock signals. In other words, said each of frequencies of said third and fourth clock signals could not be that of said first clock signals because the claim 5 recites the limitations "generating said first clock signal, said second clock signal with a period equal to a predetermined multiple of the period of said first clock signal" and "generating said third clock signal and said fourth clock signal with a period equal to another predetermined multiple of the period of said third clock signal" in lines 5-13. The Examiner assumes the limitation "said each of frequencies of said third and fourth clock signals is at least equal to that of said first clock signals" in light of the specification for the purpose of the claim rejection based on a prior art.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-5, 8, 9 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 1, 2, 4, 9 and 12 recite the limitation "the basis of execution of instructions by said central processing unit" in lines 6-7 of claims 1 and 9, in lines 5-6 of claims 2 and 4, in lines 7-8 of claim 12, respectively. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the basis" could be considered as --a basis-- since it is not clearly defined in the claims.

The claims 3 and 5 recite the limitation "the period of said first clock signal " in lines 6-7, respectively. There is insufficient antecedent basis for this limitation in the claims, respectively. Therefore, the term "the period of said first clock signal" could be considered as --a period of said first clock signal-- since it is not clearly defined in the claims, respectively.

The claim 4 recites the limitation "said synchronous clock signal of said external bus interface control circuit" in lines 14-15. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "said synchronous clock signal" could be considered as --a synchronous clock signal-- since it is not clearly defined in the claims.

The claim 4 recites the limitation "said first clock signal " in line 16. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "said first clock signal" could be considered as --a first clock signal-- since it is not clearly defined in the claims.

The claim 4 recites the limitation "said second clock signal" in lines 21-22. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "said second clock signal" could be considered as --a second clock signal-- since it is not clearly defined in the claims.

The claim 5 recites the subject matter "said semiconductor chip" in lines 16-17. There is insufficient antecedent basis for this subject matter in the claim. Therefore, the term "said semiconductor chip" could be considered as --a semiconductor chip-- since it is not clearly defined in the claims.

The claim 5 recites the subject matter "said each of frequencies of third and fourth clock signals" in lines 18-19. There is insufficient antecedent basis for this subject matter in the claim. Therefore, the

term "said each of frequencies of third and fourth clock signals" could be considered as --each of frequencies of third and fourth clock signals-- since it is not clearly defined in the claims.

The claims 8 and 9 recite the subject matter "said microprocessor chip" in the claims. There is insufficient antecedent basis for this limitation in the claims. Therefore, the subject matter "a processor chip" in line 4 of the claim 8 could be considered as --a microprocessor chip-- for the purpose of the claim rejection based on a prior art.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kume et al. [JP 405341872 A; cited by the Applicants; hereinafter Kume].

Referring to claims 1 and 2, Kume discloses a microprocessor (i.e., microprocessor 1 of Fig. 1) comprising: a central processing unit (i.e., central processing unit 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions); and an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) which controls an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) on a basis of execution of instructions by said central processing unit (i.e., a basis of external access operation by said central processing unit; See col. 4, para. [0021]), wherein said external bus interface control circuit is capable of selecting one of a plurality of external device select signals corresponding to an external access address and activating said selected external device select signal, i.e., said external bus

interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address (See col. 5, para. [0029] and [0030]), and wherein said microprocessor further comprises a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1), for controlling an operation to switch a synchronous clock signal of said external bus interface control circuit in accordance with said external device select signal activated by said external bus interface control circuit, i.e., switching said synchronous clock signal to a first clock signal in accordance with activation of said first external device select signal or to a second clock signal in accordance with activation of said second external device select signal (See col. 5, para. [0024]). However, the recitation in the preamble of the claim 1, that "a microprocessor built on a semiconductor chip" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *See Kropa v. Robie, 88 USPQ 478 (CCPA 1951).*

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner

to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] as applied to claims 1 and 2 above, and further in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 3, Kume discloses all the limitations of the claim 3 including a clock pulse generator (i.e., clock generator 30 and counting down circuit 19 in Fig. 1) and clock output pin (i.e., pin for clock signal line 21 in Fig. 1), wherein said clock pulse generator generates said first clock signal and said second clock signal (i.e., generating clock signals whose frequencies are different; See col. 5, para. [0023]), and wherein said clock output pin supply said first and second clock signals generated by said clock pulse generator to outside (See col. 5, para. [0024]), except that does not teach said clock pulse generator generates said second clock signal with a period equal to a predetermined multiple of a period of said first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio, and clock output pins supply respectively said first and second clock signals generated by said clock pulse generator in parallel to respectively outside.

Yanagiuchi discloses a clock signal generating system (Fig. 1) comprising a clock pulse generator (i.e., clock generator 1 of Fig. 1) and a clock switching control circuit (i.e., clock selector 2 of Fig. 1), wherein said clock pulse generator generates a second clock signal (e.g., clock output from $X_{½}$ 12-2 in Fig. 1) with a period equal to a predetermined multiple (i.e., ½ times multiple) of a period of a first clock signal (i.e., clock output from X_2 11-2 in Fig. 1) where said predetermined multiple is defined as a quantity equal to a frequency-division ratio (i.e., dividing factor; See col. 3, line 65 through col. 4, line 8), and clock output pins (i.e., clock signal output lines from said clock generator 1 in Fig. 1) supply respectively said first and second clock signals generated by said clock pulse generator in parallel to respectively outside (See col. 3, lines 26-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Blomgren et al. [US 5,381,543 A; hereinafter Blomgren].

Referring to claim 4, Kume discloses a microprocessor comprising: Kume discloses a microprocessor (i.e., microprocessor 1 of Fig. 1) comprising: a central processing unit (i.e., central processing unit 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions); and an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) controlling an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) on a basis of execution of instructions by said central processing unit (i.e., a basis of external access operation by said central processing unit; See col. 4, para. [0021]), wherein said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address (See col. 5, para. [0029] and [0030]), wherein said microprocessor further comprises a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1), said clock switching control circuit is capable of controlling to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal (e.g., clock signal 21 for the external data processing device 22 in Fig. 2) as well as switch a

synchronous clock signal of said central processing unit to said first clock signal (i.e., clock signal 52 for CPU 2 in Fig. 1, which is coincided with said clock signal 21 for the external data processing device 22 in Fig. 2) in response to activation of said first external device select signal, and is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to a second clock signal (e.g., clock signal 21 for the external data processing device 23 in Fig. 2) as well as switch said synchronous clock signal of said central processing unit to said second clock signal (i.e., clock signal 52 for CPU 2 in Fig. 1, which is coincided with said clock signal 21 for the external data processing device 23 in Fig. 2) in response to activation of said second external device select signal, i.e., switching said synchronous clock signal to a first clock signal in accordance with activation of said first external device select signal or to a second clock signal in accordance with activation of said second external device select signal (See col. 5, para. [0024]).

Kume does not teach said clock switching control circuit is capable of supplying a third clock signal to said central processing unit as well as supplying said first clock signal, and is capable of supplying a fourth clock signal to said central processing unit as well as supplying said second clock signal.

Blomgren discloses a dual clock mechanism (i.e., clock 422, PLL 402 and write back cache 420C, Bus Converter 420D and their signal connections in Fig. 4), wherein said dual clock mechanism is capable of supplying a third clock signal (e.g., 66MHz in Fig. 4) to a central processing unit (i.e., CPU 420A of Fig. 4) as well as supplying a first clock signal (i.e., 33MHz in Fig. 4), and is capable of supplying a fourth clock signal (e.g., other frequency 300MHz) to said central processing unit as well as supplying a second clock signal (i.e., 150MHz; See col. 7, lines 8-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dual clock mechanism, as disclosed by Blomgren, in said microprocessor, as disclosed by Kume, for the advantage of providing a means for operating said central processing unit (i.e.,

CPU) in said microprocessor (i.e., single chip microprocessor) at a multiple of the cycle speed of a memory bus (See Blomgren, col. 2, lines 30-32).

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Blomgren [US 5,381,543 A] as applied to claim 4 above, and further in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 5, Kume, as modified by Blomgren, discloses all the limitations of the claim 5 including a clock pulse generator (i.e., clock generator 30 and counting down circuit 19 in Fig. 1; Kume) and clock output pin (i.e., pin for clock signal line 21 in Fig. 1; Kume), wherein said clock pulse generator generates said first clock signal, said second clock signal (i.e., generating clock signals whose frequencies are different; See Kume, col. 5, para. [0023]), said third clock signal, said fourth clock signal (See Blomgren, col. 7, lines 8-14), and wherein said clock output pin supply said first and second clock signals generated by said clock pulse generator to outside (See Kume, col. 5, para. [0024]), except that does not teach said clock pulse generator generates said second clock signal with a period equal to a predetermined multiple of a period of said first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio, said fourth clock signal with a period equal to another predetermined multiple of a period of said third clock signal where said other predetermined multiple is defined as a quantity equal to another frequency-division ratio, wherein clock output pins supply respectively said first and second clock signals generated by said clock pulse generator to respectively outside a semiconductor chip, and wherein said each of frequencies of said third and fourth clock signals is at least equal to that of said first clock signals.

Yanagiuchi discloses a clock signal generating system (Fig. 1) comprising a clock pulse generator (i.e., clock generator 1 of Fig. 1) and a clock switching control circuit (i.e., clock selector 2 of Fig. 1), wherein said clock pulse generator generates a second clock signal (e.g., clock output from $X_{1/2}$ 12-2 in Fig. 1) with a period equal to a predetermined multiple (i.e., 1/2 times multiple) of a period of a first clock signal

(i.e., clock output from X_2 11-2 in Fig. 1) where said predetermined multiple is defined as a quantity equal to a frequency-division ratio (i.e., dividing factor; See col. 3, line 65 through col. 4, line 8), and clock output pins (i.e., clock signal output lines from said clock generator 1 in Fig. 1) supply respectively said first and second clock signals generated by said clock pulse generator in parallel to respectively outside a semiconductor chip (i.e., clock generator 1 of Fig. 1; See col. 3, lines 26-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, as modified by Blomgren, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

Thus, Kume, as modified by Blomgren and Yanagiuchi, impliedly suggests said fourth clock signal with a period equal to another predetermined multiple of a period of said third clock signal where said other predetermined multiple is defined as a quantity equal to another frequency-division ratio, and each of frequencies of a third and fourth clock signals is at least equal to that of the frequency of said first clock signal (See Blomgren, col. 7, lines 8-14; i.e., wherein in fact that other frequencies could be used for said clock signals, and other multiples could be used for said multipliers implies that said fourth clock signal with a period equal to another predetermined multiple of a period of said third clock signal where said other predetermined multiple is defined as a quantity equal to another frequency-division ratio, and each of frequencies of a third and fourth clock signals is at least equal to that of the frequency of said first clock signal).

14. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] as applied to claims 1 and 2 above, and further in view of Fujita [US 6,529,083 B2].

Referring to claim 6, Kume discloses all the limitations of the claim 6 except that does not teach said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and wherein said clock switching control circuit is further capable of controlling to switch said first clock signal after an acknowledgment of a request for suspending of said instruction execution.

Fujita discloses a clock control circuit (See Abstract), wherein a clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1) requests a central processing unit to suspend execution of instructions in response to activation of a selected external device select signal (i.e., starting the processing for changing the clocks; See col. 8, lines 10-21), and wherein said clock switching control circuit is further capable of controlling to switch a first clock signal (See col. 9, lines 25-32) after an acknowledgment of a request for suspending of said instruction execution (See col. 17-24; i.e., wherein in fact that the clock state control circuit stops the operation once, and enters the sleeping state implies that said capability of controlling to switch a first clock signal after an acknowledgment of a request for suspending of said instruction execution. In other words, the clock state control circuit is waiting for the CPU acknowledgement of a request for stopping the operation during the sleeping state).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock state control circuit, as disclosed by Fujita, in said clock switching control circuit, as disclosed by Kume, for the advantage of reducing complication in control over operating clock in said clock switching control circuit (i.e., clock control circuit) and realizing more precise and accurate control over an operating speed (See Fujita, col. 10, lines 57-60).

Referring to claim 7, Fujita teaches said clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1) is capable of controlling to switch said first clock signal at a timing synchronized with periods of said second clock signal (See col. 9, lines 33-54).

15. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 8, Kume discloses a semiconductor module (i.e., multiprocessor system in Fig. 2) on a module substrate (e.g., PCB in said multiprocessor system) including a plurality of external connection electrodes (i.e., a plurality of connectors for connecting among Data Bus 9, System Address Bus 10, microprocessor 1, the first external data processing device 22, the second external data processing device 23, etc. in Fig. 2) and a plurality of wiring layers (i.e., a plurality of PCB routing layers for the plural signals of Buses, Devices and Clock) comprising: a microprocessor chip (i.e., microprocessor 1 of Fig. 2); and a memory chip (i.e., the first external data processing device 22 of Fig. 2) operating synchronously with a first clock signal (i.e., clock signal for the first external data processing device, e.g., fast memory device), wherein said microprocessor chip includes a clock pulse generator (i.e., clock generator 30 and counting down circuit 19 in Fig. 1) for generating said first clock signal and a second clock signal (i.e., clock signal for the second external data processing device, e.g., slow memory device) with a frequency lower than said first clock signal (i.e., the second clock being slower than the first clock signal), wherein said microprocessor chip is capable of making an access to said memory chip (i.e., the first external data processing device) synchronously with said first clock signal (See col. 5, para. [0025]), and wherein said microprocessor chip is capable of making an external access to outside of said microprocessor chip through one of external connection electrodes (i.e., an external access through the external data bus 9 and the external system address bus 10 to the second external data processing device 23 in Fig. 2) synchronously with said second clock signal (See col. 5, para. [0025]).

Kume does not teach clock output pins for supplying in parallel said first and second clock signals to outside.

Yanagiuchi discloses a clock signal generating system (Fig. 1) comprising a clock pulse generator (i.e., clock generator 1 of Fig. 1) and a clock switching control circuit (i.e., clock selector 2 of Fig. 1), wherein

clock output pins (i.e., clock signal output lines from said clock generator 1 in Fig. 1) supplying in parallel a first clock signal and a second clock signal generated by said clock pulse generator to outside (See col. 3, lines 26-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

Referring to claim 9, Kume teaches said microprocessor chip (i.e., microprocessor 1 of Fig. 1) comprises: a central processing unit (i.e., CPU 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions); and an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) for controlling an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) on a basis of execution of instructions by said central processing unit (i.e., a basis of external access operation by said central processing unit; See col. 4, para. [0021]), wherein said central processing unit and said external bus interface control circuit are built in a single chip (See Fig. 1; i.e., said microprocessor 1 implementing CPU 2 and components for external bus interface control in Fig. 1), wherein said external bus interface control circuit is capable of activating a memory chip select signal for selecting said memory chip (i.e., the first external processing device 22 of Fig. 2) in response to an external access address and an external device select signal for selecting a device (i.e., the second external processing device 23 of Fig. 2)

connected to said microprocessor chip through one of said external connection electrodes (i.e., an external access through the external data bus 9 and the external system address bus 10 to the second external data processing device 23 in Fig. 2), i.e., said external bus interface control circuit is capable of activating either a memory chip select signal (i.e., the first external processing device selection) or a second external device select signal (i.e., the second external processing device selection) corresponding to an external access address (See col. 5, para. [0029] and [0030]), wherein said microprocessor chip comprises a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1), wherein said clock switching control circuit is capable of controlling to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal in response to activation of said memory chip select signal, or is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to a second clock signal in response to activation of said device select signal, i.e., switching said synchronous clock signal to a first clock signal in accordance with activation of said memory chip select signal or to a second clock signal in accordance with activation of said device select signal (See col. 5, para. [0024]).

16. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of what was well known in the art, as exemplified by Tymchenko [US 6,026,231 A].

Referring to claim 10, Kume discloses a data-processing system (i.e., multiprocessor system in Fig. 2) comprising: a first clock wire (i.e., clock wire 21 to the first external data processing device 22 in Fig. 2) for transferring a first clock signal (i.e., clock signal for the first external data processing device, e.g., fast memory device); a second clock wire (i.e., clock wire 21 to the second external data processing device 23 in Fig. 2) for transferring a second clock signal (i.e., clock signal for the second external data processing device, e.g., slow memory device) with a frequency lower than said first clock signal (i.e., the second clock being slower than the first clock signal); a first device (i.e., the first external data processing

device 22 of Fig. 2) operating synchronously with said first clock signal applying through said first clock wire; a second device (i.e., the second external data processing device 23 of Fig. 2) operating synchronously with said second clock signal (See col. 5, para. [0025]); and a third device (i.e., microprocessor 1 of Fig. 2) capable of controlling accesses to said first device synchronously with said first clock signal and capable of controlling accesses to said second device synchronously with said second clock signal (See col. 5, para. [0029] and [0030]).

Kume does not expressly teach said first clock wire, said second clock wire, said first device, said second device and said third device are provided on a mounting board.

The Examiner takes Official Notice that said first clock wire, said second clock wire, said first device, said second device and said third device are provided on a mounting board (e.g., PCB board), is well known to one of ordinary skill in the art of data processing system, as evidenced by Tymchenko (See Fig. 1 and col. 2, lines 63+; i.e., wherein in fact that a plurality of oscillator output wires (i.e., a first clock wire, a second clock wire, etc.), a plurality of CPUs and Memories (i.e., a first device, a second device, and a third device, etc.) are provided on a computer system 10 in Fig. 1(i.e., a mounting board) suggests said first clock wire, said second clock wire, said first device, said second device and said third device are provided on a mounting board).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said first clock wire, said second clock wire, said first device, said second device and said third device on a mounting board (e.g., computer system mother board) since it would improve the reliability of said data-processing system.

Referring to claim 11, Kume discloses all the limitations of the claim 11including said mounting board comprising a first circuitry (i.e., microcomputer in Fig. 2) including a first board wire (i.e., Data Bus 9 of Fig. 2) connected to said second device (i.e., the second external device 23 of Fig. 2); and a second circuitry (i.e., microprocessor 1 of Fig. 2) including a second board wire (i.e., Data Bus 7 of Fig.

1) connected to said first board wire (i.e., Data Bus 9 of Fig. 1) and said second board wire is connected to said first device (i.e., connected to the first external device 22 through said Data Bus 9 in Fig. 2) and a third device (i.e., connected to microprocessor 1 in Fig. 1) except that does not expressly teach said first circuitry is implemented on a circuit board, i.e., a first circuit board, and said second circuitry is implemented on another circuit board, i.e., a second circuit board.

The Examiner takes Official Notice that said first circuitry being implemented on a first circuit board, and said second circuitry being implemented on a second circuit board, is well known to one of ordinary skill in the art of data processing system, as evidenced by Tymchenko (See Fig. 1 and col. 2, lines 63+; i.e., wherein in fact that a plurality of CPU modules (i.e., a first circuitry and a second circuitry) are implemented on a plurality of CPU boards (i.e., circuit board)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented each of said first circuitry and said second circuitry on the respective circuit board since it would reduce the repairing/diagnostic service time when said data-processing system is in failure.

Referring to claim 12, Kume teaches said third device is a microprocessor on a single semiconductor chip (i.e., microprocessor 1 of Fig. 1) comprising a central processing unit (i.e., CPU 2 of Fig. 1) for executing instructions (See Fig. 1 and col. 5, para. [0022]; i.e., wherein in fact that the Fig. 1 shows the address bus 8 and the data bus 7 coupled to said central processing unit, and said central processing unit outputting access address inherently anticipates that said central processing unit executing instructions), an external bus interface control circuit (i.e., micro controller 15, control register 14 and clock selection logic 18 in Fig. 1) for controlling an external bus (i.e., system data bus 9 and system address bus 10 in Fig. 1) on a basis of execution of instructions by said central processing unit (i.e., a basis of external access operation by said central processing unit; See col. 4, para. [0021]), wherein said external bus interface control circuit is capable of activating a first external device select signal for

selecting said first device or a second external device select signal for selecting said second device in accordance with an external access address, i.e., said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address (See col. 5, para. [0029] and [0030]), wherein said third device (i.e., microprocessor of Fig. 1) further includes a clock switching control circuit (i.e., clock output selection switch 20 of Fig. 1), and wherein said clock switching control circuit is capable of controlling to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal in response to activation of said first external device select signal, or is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to a second clock signal in response to activation of said second external device select signal, i.e., switching said synchronous clock signal to a first clock signal in accordance with activation of said first external device select signal or to a second clock signal in accordance with activation of said second external device select signal (See col. 5, para. [0024]).

17. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] as applied to claims 10-12 above, and further in view of Yanagiuchi [US 5,684,418 A].

Referring to claim 13, Kume discloses all the limitations of the claim 13 including a clock pulse generator (i.e., clock generator 30 and counting down circuit 19 in Fig. 1) and clock output pin (i.e., pin for clock signal line 21 in Fig. 1), except that does not teach said clock pulse generator applies said first clock signal and said second clock signal with a period equal to a predetermined multiple of the period of said first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio, and wherein said clock output pins apply respectively said first and second clock signals generated by said clock pulse generator in parallel to outside said semiconductor chip.

Yanagiuchi discloses a clock signal generating system (Fig. 1) comprising a clock pulse generator (i.e., clock generator 1 of Fig. 1) and a clock switching control circuit (i.e., clock selector 2 of Fig. 1), wherein

said clock pulse generator applies a first clock signal (e.g., clock output from X_2 11-2 in Fig. 1) and a second clock signal (i.e., clock output from $X_{1/2}$ 12-2 in Fig. 1) with a period equal to a predetermined multiple of a period of said first clock signal where said predetermined multiple (i.e., 1/2 times multiple) is defined as a quantity equal to a frequency-division ratio (i.e., dividing factor; See col. 3, line 65 through col. 4, line 8), and wherein said clock output pins (i.e., clock signal output lines from said clock generator 1 in Fig. 1) apply respectively said first and second clock signals generated by said clock pulse generator in parallel to outside a semiconductor chip (i.e., clock generator 1 of Fig. 1; See col. 3, lines 26-47). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said clock generator and said clock selector in said clock signal generating system, as disclosed by Yanagiuchi, for said clock pulse generator and said clock switching control circuit, respectively, as disclosed by Kume, for the advantage of providing a clock signal generator which can make a multiplier and a frequency divider generating a frequency which is not being used stop and thereby prevent needless power consumption and achieve a low power consumption of a system or chip as whole (See Yanagiuchi, col. 1, lines 44-49).

18. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kume [JP 405341872 A] in view of Blomgren [US 5,381,543 A] as applied to claim 4 above, and further in view of Fujita [US 6,529,083 B2].

Referring to claim 14, Kume, as modified by Blomgren, discloses all the limitations of the claim 14 except that does not teach said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and wherein said clock switching control circuit is further capable of controlling to switch said first clock signal after an acknowledgment of a request for suspending of said instruction execution.

Fujita discloses a clock control circuit (See Abstract), wherein a clock switching control circuit (i.e., clock state control circuit 4 of Fig. 1) requests a central processing unit to suspend execution of instructions in

response to activation of a selected external device select signal (i.e., starting the processing for changing the clocks; See col. 8, lines 10-21), and wherein said clock switching control circuit is further capable of controlling to switch a first clock signal (See col. 9, lines 25-32) after an acknowledgment of a request for suspending of said instruction execution (See col. 17-24; i.e., wherein in fact that the clock state control circuit stops the operation once, and enters the sleeping state implies that said capability of controlling to switch a first clock signal after an acknowledgment of a request for suspending of said instruction execution. In other words, the clock state control circuit is waiting for the CPU acknowledgement of a request for stopping the operation during the sleeping state).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock state control circuit, as disclosed by Fujita, in said clock switching control circuit, as disclosed by Kume, as modified by Blomgren, for the advantage of reducing complication in control over operating clock in said clock switching control circuit (i.e., clock control circuit) and realizing more precise and accurate control over an operating speed (See Fujita, col. 10, lines 57-60).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Bus Switching,

Higaki et al. [US 5,481,679 A] disclose data processing apparatus having bus switching for selectively connecting buses to improve data throughput.

Nozuyama [US 5,862,359 A] discloses data transfer bus including divisional buses connectable by bus switch circuit.

Cepulis et al. [US 6,061,754 A] disclose data bus having switch for selectively connecting and disconnecting devices to or from the bus.

With regard to Multi-Speed Bus Operation,

Clayton, IV [US 4,476,527] discloses synchronous data bus with automatically variable data rate.

Mitsuishi et al. [US 5,774,702 A] disclose integrated circuit having function blocks operating in response to clock signals.

Lee et al. [US 6,134,621 A] disclose selection from a plurality of bus operating speeds for a processor bus interface during processor reset.

Olnowich [US 5,263,172 A] discloses multiple speed synchronous bus having single clock path for providing first or second clock speed based upon speed indication signals.

Klein [US 6,425,041 B1] discloses time-multiplexed multi-speed bus.

Kelly et al. [US 6,134,621 A] disclose variable slot configuration for multi-speed bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

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